

(Prior Art)

Figure 1

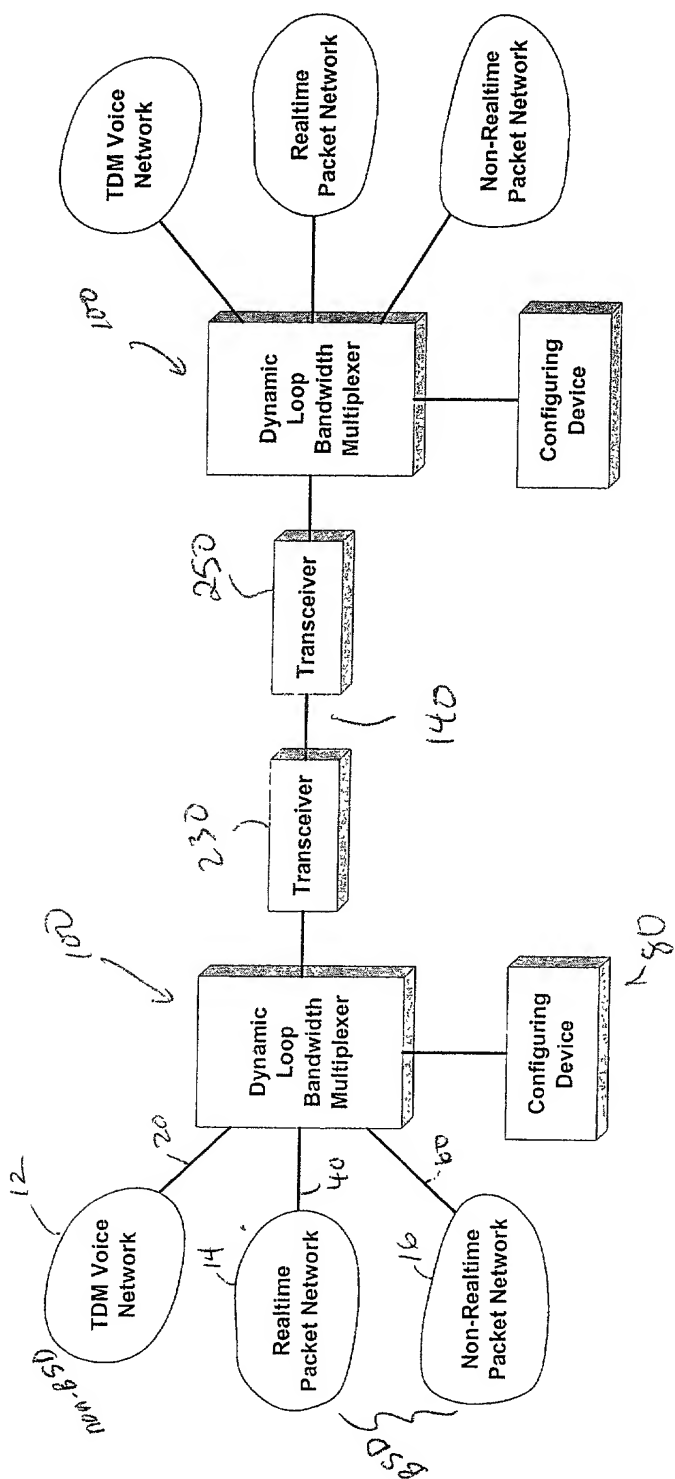


Figure 2

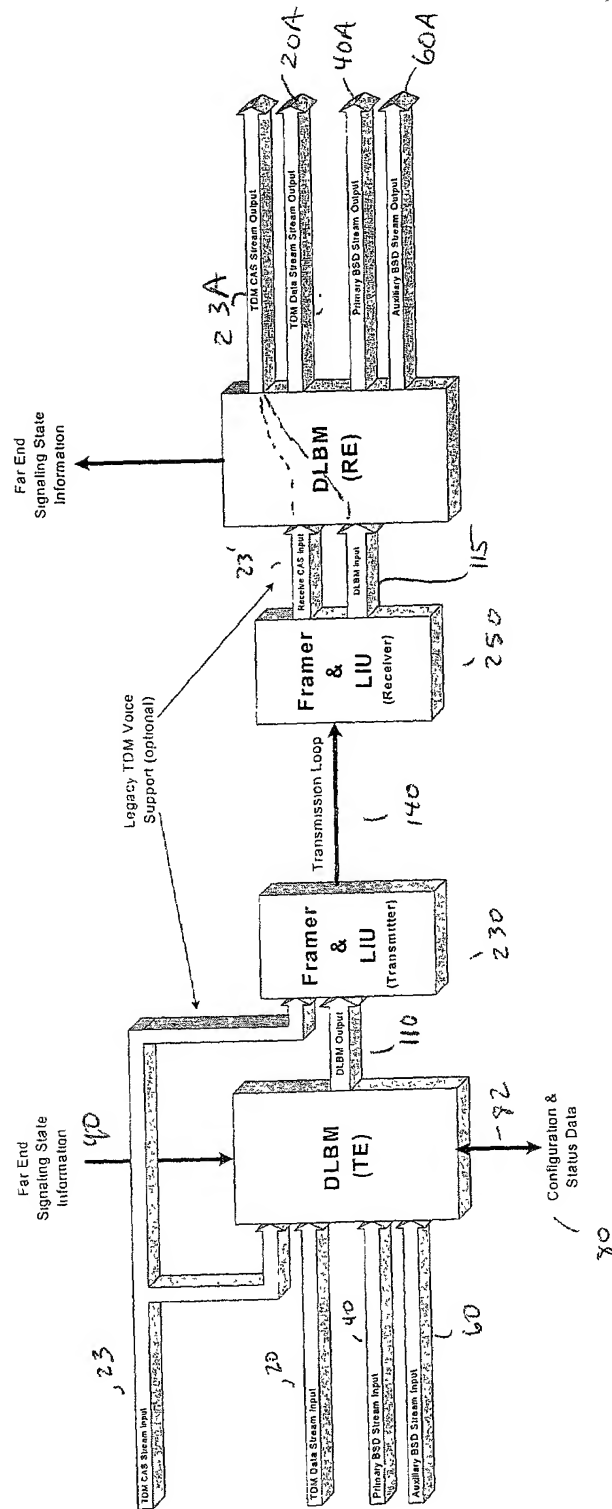


Figure 3

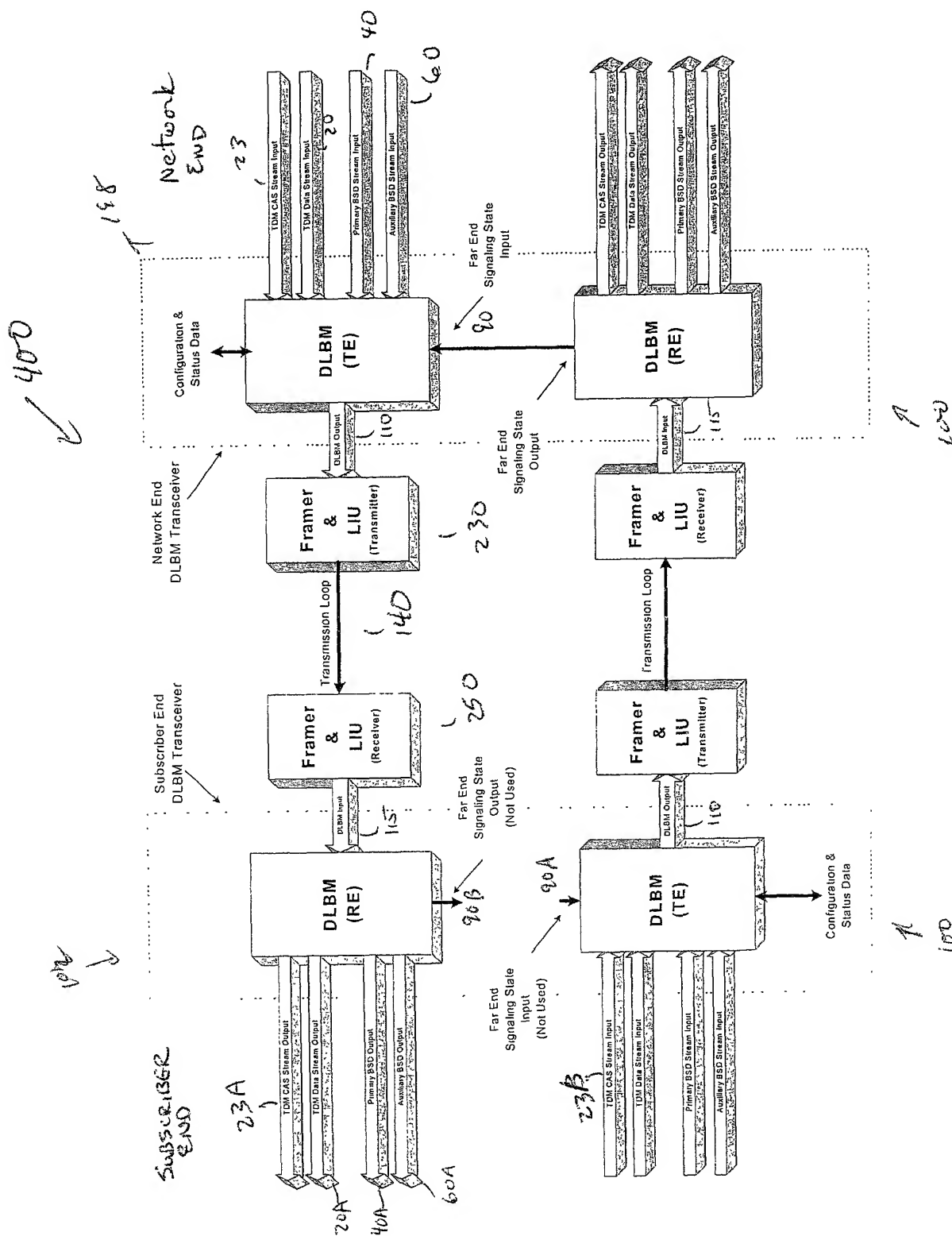


Figure 4

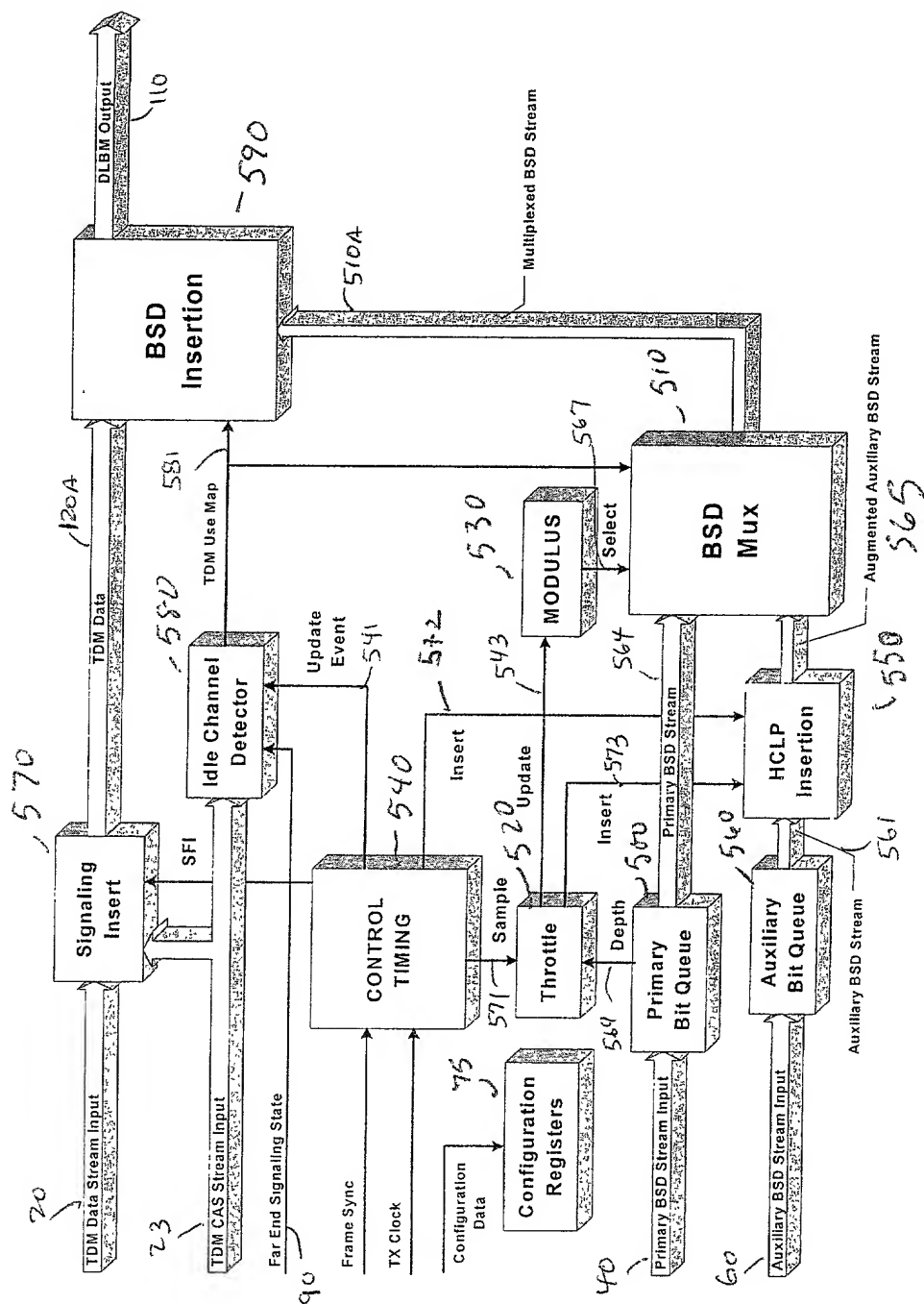


Figure 5

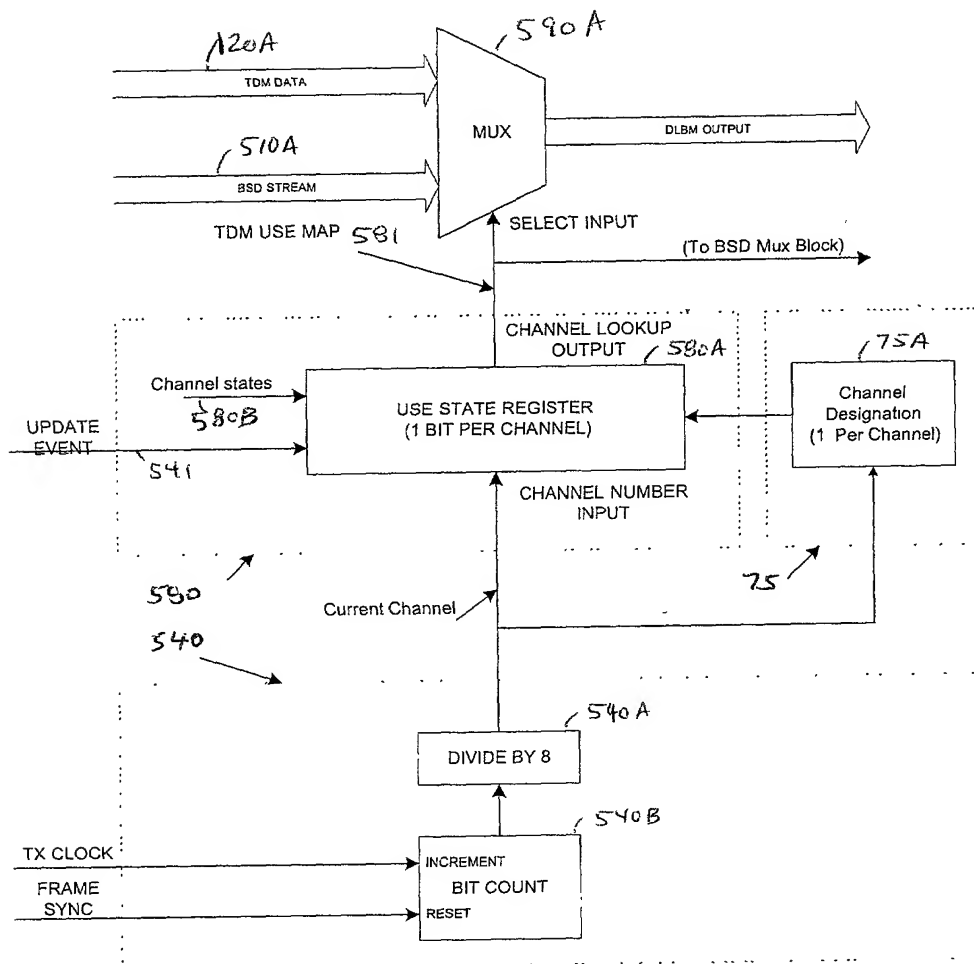
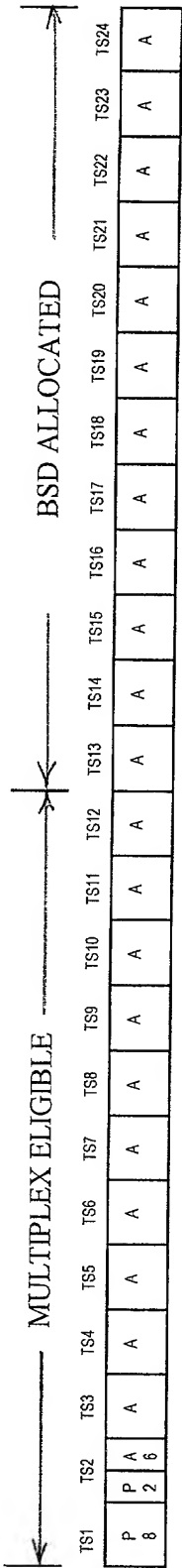
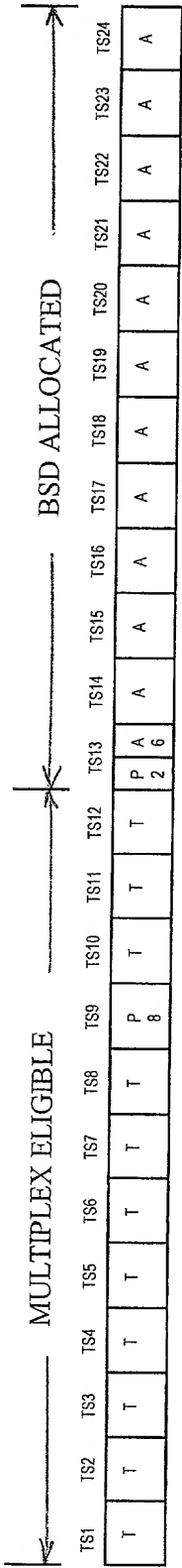


Figure 6



P = PRIMARY; A = AUXILIARY
MODULUS = 10
TS1 to TS12 = IDLE

Figure 7



P = PRIMARY; A = AUXILIARY; T = TDM
MODULUS = 10
TS1 to TS8 = ACTIVE; TS9 = IDLE; TS10 to TS12 = ACTIVE

Figure 8

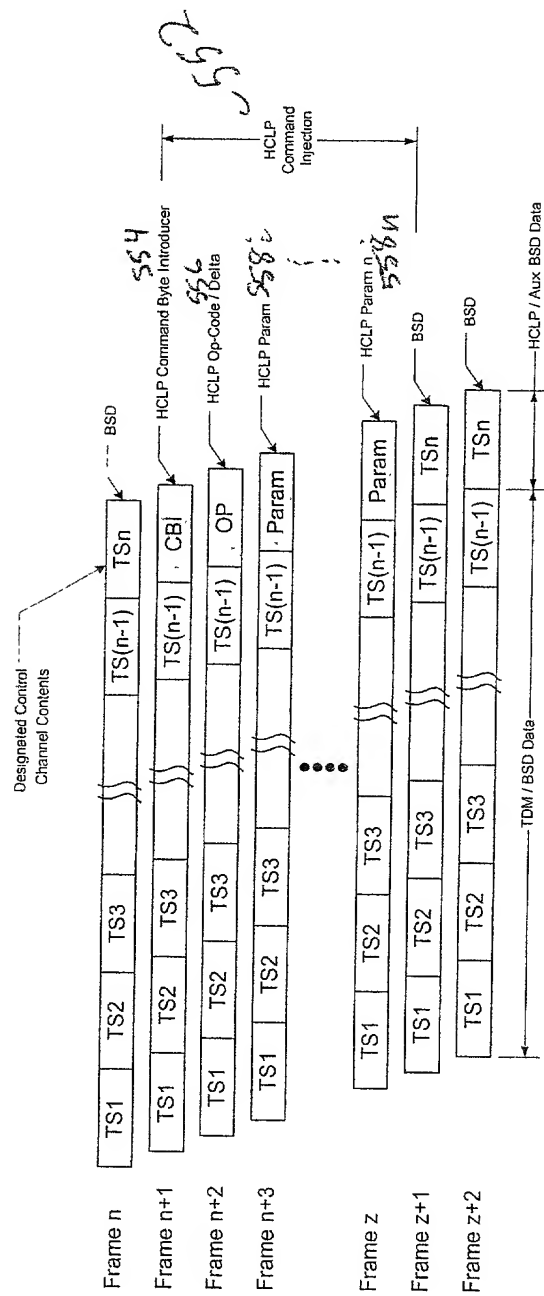


Figure 9

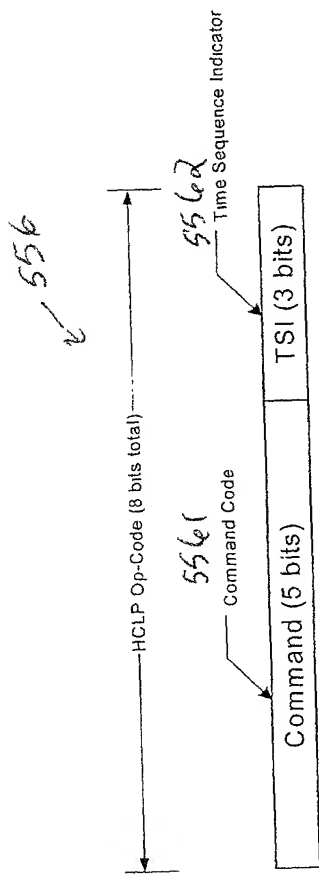


Figure 10

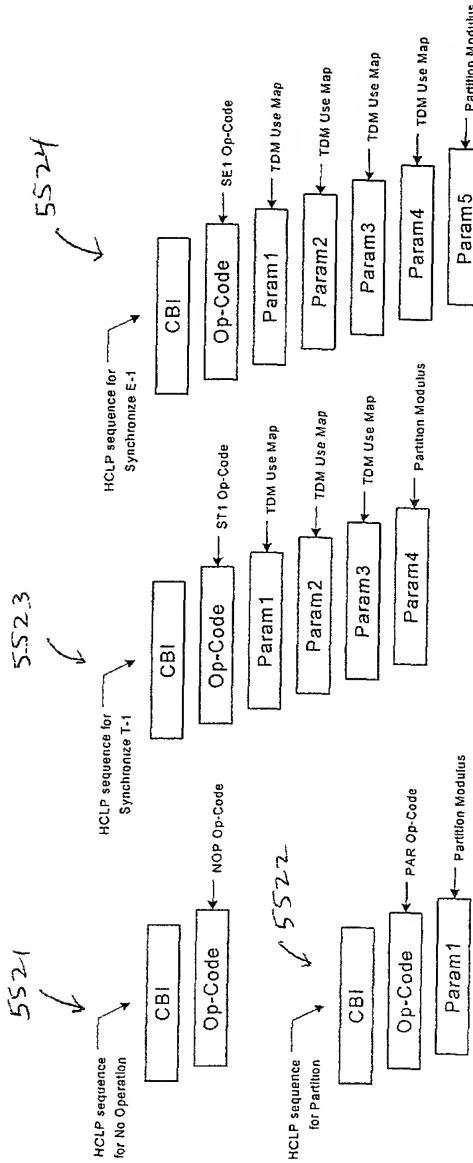


Figure 11

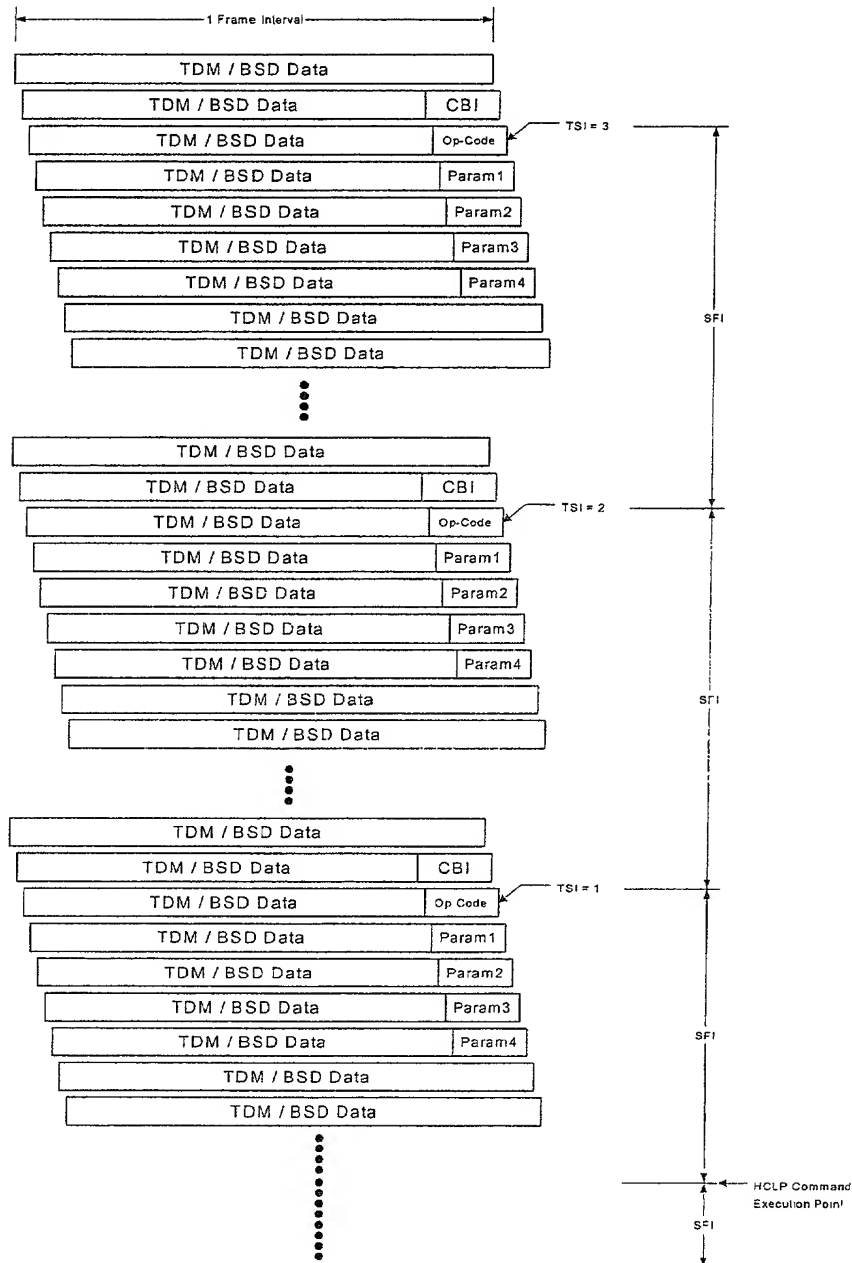


Figure 12

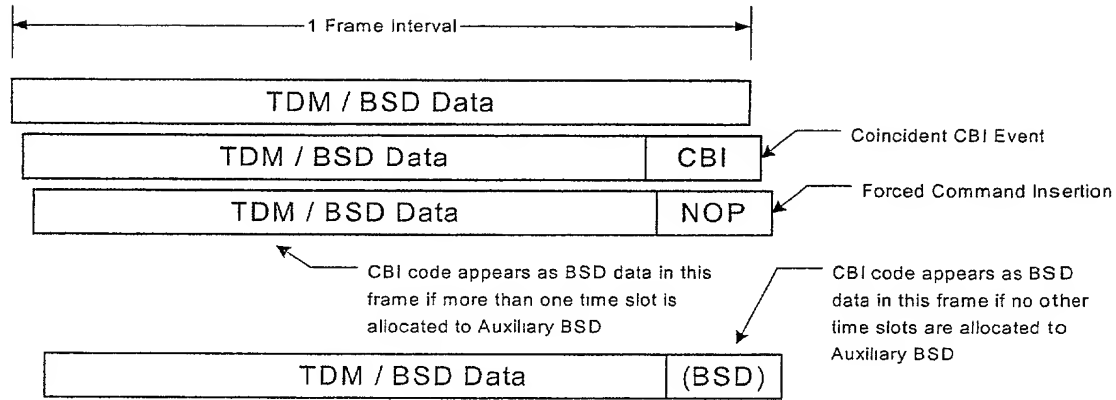


Figure 13

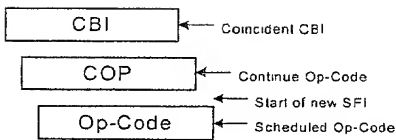


Figure 14

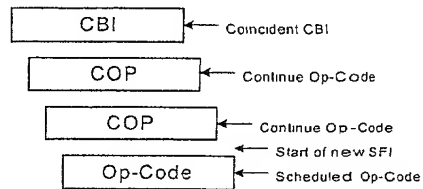


Figure 15

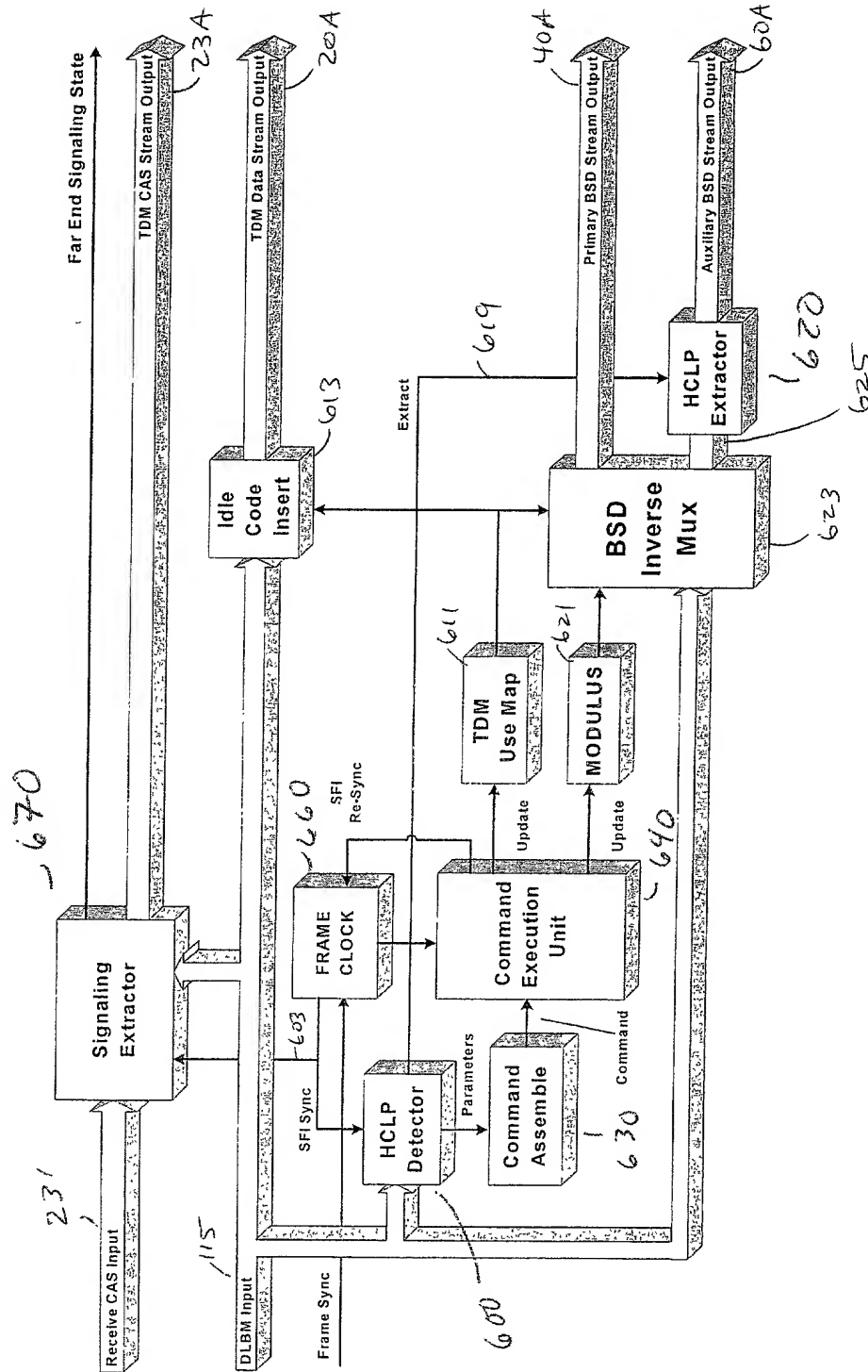


Figure 16

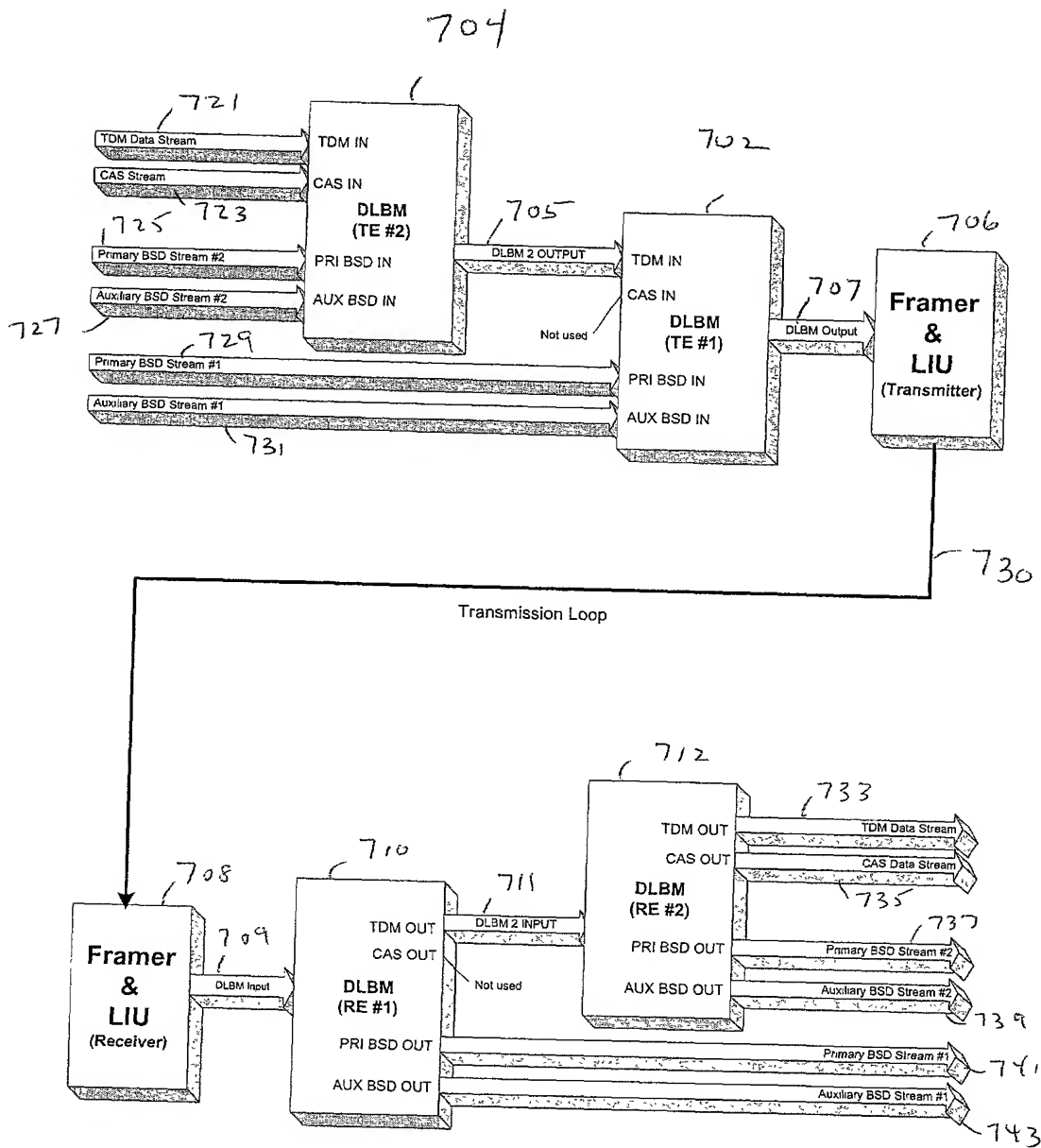


Figure 17